## REMARKS

This Amendment responds to the Office Action dated September 22, 2005 in which the Examiner rejected claims 1-3 and 5-6 under 35 U.S.C. §101 and under 35 U.S.C. §103.

As indicated above, claim 1 has been amended in order to be directed to statutory subject matter. Therefore, Applicants respectfully request the Examiner withdraws the rejection to the claims under 35 U.S.C. §101.

As indicated above, claim 1 has been amended in order to make explicit what is implicit in the claim. The amendment is unrelated to a statutory requirement for patentability.

Claim 1 claims a delay time estimation method for estimating a delay time in a logic circuit that includes a MOS transistor. The method comprises the steps of: constructing a delay library including function information for specifying a model of an Ids-Vds characteristic at a given gate potential and also includes function information related to a slew rate specifying a fixed delay, where Ids denotes a drain-source current and Vds denotes a drain-source voltage; modeling the MOS transistor by a resistive element having fixed resistance and a power source voltage that varies with time; determining an operating current characteristic thus modeled and segmenting the operating current characteristic based upon the delay library into a first region in which a current increases as a gate potential varies, a second region corresponding to a saturation region of the MOS transistor in which region the current gradually decreases as the gate potential remains constant, and a third region corresponding to a linearity region of the MOS transistor in which region the

current decreases exponentially as the gate potential remains constant; and estimating the delay time of the MOS transistor and output thereof.

Through the method of the claimed invention segmenting the operating current characteristic of a modeled MOS transistor into a plurality of regions based upon gate potential, as claimed in claim 1, the claimed invention provides a delayed time estimation method which matches the characteristic of the transistor. The prior art does not show, teach or suggest the method as claimed in claim 1.

Claims 1-3 and 5-6 were rejected under 35 U.S.C. §103 as being unpatentable over *Arunachalum et al* (CMOS gate delay models for general RLC loading, IEEE 1997) in view of *Cocchini et al* (A comprehensive submicrometer MOST delay model and its application to CMOS buffers, August 1997).

*Arunachalum et al* appears to disclose to preserve the simplicity and efficiency of the empirical gate models, a complex RC load was mapped to an "effective capacitance" in [1]. This method was used in [2] to accurately capture the shape of the output voltage for RC loads, with the gate being modeled in terms of a time varying voltage-source in series with a constant resistance (page 224, second column, lines 2-8). The way the model is used to calculate delays for RC loads is as follows: Given a reduced order model of an RC-load, an "effective capacitance" is found which would draw the same average current as the reduced order model during the period of time when the Thevenin voltage is in transition. The initial guess for this $C_{eff}$ is taken as the total capacitance of the RC load, and the Thevenin voltage parameters for that capacitance are extracted from the table or equation model. Then, equating the average currents obtained by using these Thevenin voltage parameters, a new $C_{eff}$ is computed. This iterative procedure is repeated

until convergence is obtained. Empirical results indicate good convergence properties (2 to 4 iterations are usually enough) (page 225, column 2, lines 3-16).

Thus, *Arunachalam* merely discloses generating delay models for CMOS transistors. Nothing in *Arunachalam et al.* shows, teaches or suggests segmenting an operating current characteristic into first, second and third regions based upon changes to the gate potential as claimed in claim 1. Rather, *Arunachalam* merely discloses modeling of empirical gate/cell delay models and RC load.

*Cocchini* appears to disclose an accurate delay model for MOS transistors in submicrometer CMOS digital circuits is presented. It takes into account a ramp shape input voltage and a feed-forward capacitive coupling between gate and drain nodes, along with the main second-order effects present in short-channel MOS transistors (Abstract). The input voltage $V_I$ has a ramp shape with slope $K_I$ [$Vs^{-1}$], $C_L$ is the load capacitance, and $C_{FF}$ is the feed-forward capacitance which is equal to the overlap capacitance of the transistor plus the capacitance introduced by any additional circuitry ($C_{GD}$ neglected in saturation). At t = 0, $C_L$, is charged at $V_{DD}$ and the input voltage is zero. For t > 0, the input voltage $V_I$ increases as $V_I = K_I t$ until it reaches $V_{DD}$ and then remains constant, while $V_O$, after an initial increase, decreases to reach the switching voltage $V_S = V_{DD}/2$. During the transition of $V_O$ from $V_{DD}$ to $V_S$, depending on the slope $K_I$ of the input voltage, five different regions of operation of the MOS transistor can be distinguished as shown in Fig. 2 (page 1225, column 1, lines 10-22).

Thus, *Cocchini et al.* merely discloses a delay model based upon time t and input voltage $V_I$. Nothing in *Cocchini et al.* shows, teaches or suggests segmenting the operating current characteristics into regions based upon variations in gate

potential as claimed in claim 1. Rather, *Cocchini* merely discloses a model based upon input voltage and time.

Since nothing in *Arunachalam et al.* or *Cocchini et al.* show, teach or suggest segmenting an operating current characteristic into regions based upon different gate potentials as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claims 2-3 and 5-6 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 and 5-6 would not have been obvious within the meaning of 35 U.S.C. §103 over *Arunachalum et al* and *Cocchini et al* at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 and 5 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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